REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-8 and 15-22 are pending in the present application. Claims 1, 2-4 and 7 have been amended and Claims 15-22 have been added by the present amendment.

In the outstanding Office Action, the drawings were objected to; and Claims 1-8 were rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted prior art AAPA in view of Lou.

Regarding the objection to the drawings, the outstanding Office Action indicates Figures 22-24 should be designated by a legend such as "Prior Art." Applicants note, however, that a supplemental amendment was filed on July 30, 2002, amending Figures 22-24 to be labeled "Background Art" instead of "Prior Art" to correspond with the description in the specification (see page 17, lines 16-17, for example). Further, item 2 of the outstanding Office Action indicates the drawing changes in the supplemental amendment have been approved. Accordingly, it is believed the objection to the drawings has been overcome.

Claims 1-8 stand rejected under 35 U.S.C. § 103(a) as unpatentable over AAPA in view of Lou is respectfully traversed.

The present invention introduces lifetime killers to a first semiconductor region below an isolation insulating film by a stress of a silicon nitride film, thereby suppressing a floating-body effect which is a problem inherent in an SOI structure. It is thus preferable to provide the silicon nitride film as close as possible to the isolation insulating film rather than a wiring side, so that a stress of the silicon nitride film can be efficiently introduced below the isolation insulating film.

In Lou, an oxide film below a nitride film is thinned to be close to an isolation insulating film. This shortens the distance between a metal wiring and a semiconductor substrate and as a result, a parasitic wire capacitance suddenly increases resulting in a decrease in speed performance and an increase in power consumption.

A thick insulating film having a thickness of approximately 1 μm is generally provided between a metal wire and a substrate to minimize a parasitic wire capacitance. Thus, it can be concluded Lou discloses a structure on a bulk substrate and focuses on a wire structure.

In the structure according to the present invention, a second oxide film is provided on the silicon nitride film to decrease a parasitic wire capacitance, and the silicon nitride film as well as the second oxide film play important roles. Thus, the structure disclosed by Lou focusing on a wire structure differs from the claimed semiconductor device.

Accordingly, it is respectfully submitted independent Claim 1 and each of the claims depending therefrom are allowable.

In addition, new Claims 15-22 have been added to set forth the invention in a varying scope and Applicants submit the new claims are supported by the originally filed specification. It is respectfully submitted new Claims 15-22 are allowable for similar reasons as discussed above.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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IN THE CLAIMS

--1. (Twice Amended) A semiconductor device comprising:

an SOI substrate including a substrate in which at least its surface is insulative and a semiconductor layer provided on said surface of said substrate, said semiconductor layer having a first active region of a first conductivity type and a second active region of the first conductivity type both of which are provided in a main surface thereof;

an isolation insulating film formed between said first and second active regions in said main surface of said semiconductor layer, leaving a first semiconductor region which is part of said semiconductor layer between the isolation insulating film and said surface of said substrate;

a first [interlayer insulating] oxide film formed on said first and second active regions and a surface of said isolation insulating film;

a silicon nitride film formed on said first [interlayer insulating] oxide film; [and]

a second [interlayer insulating] oxide film formed on a surface of said silicon nitride film; and

at least one wire formed on said second oxide film.

2. (Twice Amended) The semiconductor device according to claim 1, wherein said substrate includes a semiconductor substrate and a buried insulating film entirely provided on a main surface of said semiconductor substrate,

said semiconductor device further comprising:

first source region and drain region of a second conductivity type formed in said main surface of said semiconductor layer of said first active region separated from each other;

a first gate electrode so formed on said main surface of said semiconductor layer with a first gate insulating film interposed therebetween as to oppose a region sandwiched between said first source region and drain region;

a first impurity region of the first conductivity type formed in said second active region, being electrically connected to said region sandwiched between said first source region and drain region through said first semiconductor region below said isolation insulating film; and

a first wire, a second wire and a third wire connected to said first source region and drain region and said first impurity region through contact holes which are so formed as to penetrate said first and second [interlayer insulating] <u>oxide</u> films and said silicon nitride film, respectively,

<u>wherein said at least one wire includes said first to third wires</u>.

3. (Amended) The semiconductor device according to claim 2, wherein

said semiconductor layer further has a third active region of the second conductivity type and a fourth active region of the second conductivity type both of which are provided in said main surface thereof, and

said isolation insulating film is further provided between said third and fourth active regions and between said first and fourth active regions, said isolation insulating film provided between said third and fourth active regions is formed in said main surface of said semiconductor layer, leaving a second semiconductor region which is part of said semiconductor layer between itself and said buried insulating film, and said isolation insulating film provided between said first and fourth active regions is formed in said main

surface of said semiconductor layer, leaving a third semiconductor region which is part of said semiconductor layer between itself and said buried insulating film,

said semiconductor device further comprising:

second source region and drain region of the first conductivity type formed in said main surface of said semiconductor layer of said fourth active region at a predetermined distance;

a second gate electrode so formed on said main surface of said semiconductor layer with a second gate insulating film interposed therebetween as to oppose to a region sandwiched between said second source region and drain region; and

a second impurity region of the second conductivity type formed in said main surface of said semiconductor layer of said third active region, being electrically connected to said region sandwiched between said second source region and drain region through said second semiconductor region below said isolation insulating film,

wherein said first [interlayer insulating] oxide film, said silicon nitride film and said second [interlayer insulating] oxide film extend onto said main surface of said semiconductor layer in said third and fourth active regions,

said semiconductor device further comprising:

a fourth wire, a fifth wire and a sixth wire connected to said second source region and drain region and said second impurity region through said contact holes which are formed in said first and second [interlayer insulating] oxide films and said silicon nitride film, respectively.

4. (Amended) The semiconductor device according to claim 2, wherein

said semiconductor layer further has a third active region of the second conductivity type and a fourth active region of the second conductivity type both of which are provided in said main surface thereof, and

said isolation insulating film is further provided between said third and fourth active regions and between said first and fourth active regions, said isolation insulating film provided between said third and fourth active regions is formed in said main surface of said semiconductor layer, leaving a second semiconductor region which is part of said semiconductor layer between itself and said buried insulating film, and said isolation insulating film provided between said first and fourth active regions is so formed as to reach said buried insulating film,

said semiconductor device further comprising:

second source region and drain region of the first conductivity type formed in said main surface of said semiconductor layer of said fourth active region at a predetermined distance;

a second gate electrode so formed on said main surface of said semiconductor layer with a second gate insulating film interposed therebetween as to oppose to a region sandwiched between said second source region and drain region; and

a second impurity region of the second conductivity type formed in said main surface of said semiconductor layer of said third active region, being electrically connected to said region sandwiched between said second source region and drain region through said second semiconductor region below said isolation insulating film,

wherein said first [interlayer insulating] <u>oxide</u> film, said silicon nitride film and said second [interlayer insulating] <u>oxide</u> film extend onto said main surface of said semiconductor layer in said third and fourth active regions,

said semiconductor device further comprising:

[wires] a fourth, a fifth and a sixth wire connected to said second source region and drain region and said second impurity region through said contact holes which are formed in said first and second [interlayer insulating] oxide films and said silicon nitride film, respectively.

7. (Twice Amended) The semiconductor device according to claim 1, wherein said silicon nitride film includes a silicon nitride film entirely formed on said first [interlayer insulating] oxide film except a portion where contact holes are formed.

15-22. (New).--